

We claim:

- 1 1. A circuit arrangement for rapidly switching a load, in particular an inductive load, comprising:
  - 3 - a switching transistor implemented as an N-channel MOS power transistor and connected as a high-side switch for connecting a load with a supply voltage,
  - 5 - controllable switching means for applying a potential exceeding the voltage 6 of the supply voltage source to the gate electrode of the switching transistor, wherein 7 said switching means incorporate at least a first switching-means transistor whose 8 collector current can flow at least in part to the gate electrode of the switching 9 transistor during the ON state, and wherein the first switching-means transistor is 10 connected as a current source.
- 1 2. The circuit arrangement according to Claim 1, wherein the first switching- 2 means transistor connected as a current source is part of a current mirror circuit.
- 1 3. The circuit arrangement according to Claim 2, wherein the current mirror 2 circuit additionally incorporates a first current mirror resistor and a second current 3 mirror resistor each connected to a low voltage source on the one hand and the first 4 current mirror resistor being connected to the base electrode and the current mirror 5 resistor being connected to the emitter electrode of the first switching-means transistor 6 on the other.
- 1 4. The circuit arrangement according to Claim 2, wherein the first switching- 2 means transistor is a pnp transistor.
- 1 5. The circuit arrangement according to Claim 1, wherein the collector current of 2 the first switching-means transistor flows to the gate electrode of the switching 3 transistor via a diode connected in the flow direction.

- 1    6.     The circuit arrangement according to Claim 2, wherein the ratio of the  
2     resistance values of the first current mirror resistor and the second current mirror  
3     resistor corresponds to approximately 100:1.
  
- 1    7.     The circuit arrangement according to Claim 2, wherein an input current of the  
2     current mirror circuit is controllable by means of a second switching-means transistor  
3     connected as a current source and clocked by a control signals.
  
- 1    8.     The circuit arrangement according to Claim 7, wherein the input current of the  
2     current mirror flows to the latter via an RC element comprising an RC element resistor  
3     and a parallel-connected RC element capacitor.
  
- 1    9.     The circuit arrangement according to Claim 8, wherein the time constant of the  
2     RC element is so designed that the RC element-capacitor is not charged significantly  
3     during the turn-on time of the switching transistor, but virtually completely charged  
4     during its ON time.
  
- 1    10.    The circuit arrangement according to Claim 2, wherein the current mirror  
2     circuit further includes a diode connected in series with the first current mirror resistor  
3     in and in the flow direction of the current mirror input current.
  
- 1    11.    The circuit arrangement according to Claim 1, wherein a bootstrap capacitor is  
2     provided which is connected to the low voltage source on the one hand and to the  
3     source electrode of the switching transistor on the other.
  
- 1    12.    The circuit arrangement according to Claim 3, wherein there is provided a  
2     bootstrap diode oriented in the forward direction for coupling the voltage of the low  
3     voltage source into the current mirror circuit.
  
- 1    13.    The circuit arrangement according to Claim 3, wherein the low voltage source  
2     has an auxiliary voltage source sitting on top of the potential of the supply voltage.

- 1    14.   The circuit arrangement according to Claim 1, wherein a third switching-  
2    means transistor is provided whose emitter electrode is connected to the gate electrode  
3    of the switching transistor and whose collector electrode is connected via a leakage  
4    resistor to the source electrode of the switching transistor.
  
- 1    15.   The circuit arrangement according to Claim 14, wherein the base electrode of  
2    the third switching-means transistor is connected via a leakage resistor to the source  
3    electrode of the switching transistor.
  
- 1    16.   The circuit arrangement according to Claim 14, wherein the third switching-  
2    means transistor is a pnp transistor.
  
- 1    17.   The circuit arrangement according to Claim 5, wherein a third switching-  
2    means transistor is provided whose emitter electrode is connected to the gate electrode  
3    of the switching transistor and whose collector electrode is connected via a leakage  
4    resistor to the source electrode of the switching transistor, and wherein the diode via  
5    which the collector current of the first switching-means transistor flows to the gate  
6    electrode of the switching transistor is disposed between the collector of the first  
7    switching-means transistor and the emitter of the second switching-means transistor.

1    18. A method for rapidly switching a load, in particular an inductive load,  
2    comprising the steps of:

3                 - connecting a load via a switching transistor implemented as an N-channel  
4    MOS power transistor with a supply voltage,

5                 - applying a potential exceeding the voltage of the supply voltage source to the  
6    gate electrode of the switching transistor through switching means, wherein said  
7    switching means incorporate at least a first switching-means transistor whose collector  
8    current can flow at least in part to the gate electrode of the switching transistor during  
9    the ON state, and wherein the first switching-means transistor is connected as a  
10   current source.

1    19. The method according to Claim 18, wherein the collector current of the first  
2    switching-means transistor flows to the gate electrode of the switching transistor via a  
3    diode connected in the flow direction.

1    20. The method according to Claim 18, further comprising the step of providing a  
2    third switching-means transistor whose emitter electrode is connected to the gate  
3    electrode of the switching transistor and whose collector electrode is connected via a  
4    leakage resistor to the source electrode of the switching transistor.